RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, DECEMBER 2015 FIRST YEAR [BATCH 2015-18] COMPUTER SCIENCE [Hons]

Date : 14/12/2015

[Use a separate Answer Book for each Group]

Group - A

Answer <u>any one</u> question: [1×5]]
1. Draw a flowchart or give an algorithm to output twin primes within the range 1 to 100. Twin primes are two prime numbers that differs by 2. [5]]
2. a) Prove that, the function $F(A, B, C) = \overline{A}BC + A\overline{B} + \overline{B}\overline{C}$ is functionally complete. [2]]
b) Build a Binary Decision Diagram (BDD) for the function $f(a,b,c,d) = abc + \overline{b}d + \overline{c}d$ with variable ordering $b \le c \le d \le a$.]
Answer <u>any two</u> questions: [2×10]]
 3. a) Obtain Disjunctive Normal Form (DNF) of the following: P⇒((p⇒q) ∧ ~ (~ q ∨ ~ p)). b) Prove the transposition theorem of boolean algebra using boolean laws and axioms. c) Establish the following relationship: 2^r ≥ d+r+1, where r is the number of redundant bits and d is the number of data bits in Hamming code. d) What is the advantage of Quine-McCluskey method over K-map method?]
4. a) Discuss the validity of the following argument: "All graduates are educated. Ram is a graduate. Therefore, Ram is educated." [4]	
b) Find the value of N in the following expression. $(345)_6 + (632)_7 + (487)_9 = (N)_5$. [3]]
c) Find all possible solutions of the following equation $(43)_x = (y3)_8$, where x and y are unknown. [3]]
 5. a) What do you mean by well-formed formula (WFF)? When a WFF is said to be valid? b) Show that the WFF's i) p→q (p implies q)]
and ii) $\sim p \vee q$ are equivalent. [3]]
c) Find the minimal SOP (Sum of Product) expression for $\sum m(6,7,8,9) + d(10,11,12,13,14,15)$ using binary designations of minterms in Quine-McCluskey method. [4]	
6. a) Perform the following subtraction in 8421 BCD code using 10's complement method. 2064-507.6.]
b) Obtain canonical Product of Sum (POS) form of the following boolean function : $F = (p+r)(\overline{q}+p)(\overline{p}+q) \ . \ [3]$]
c) Show that the dual of Exlusive – OR is equal to its complement. d) 'Hamming Code is single bit error correction scheme' —Justify. [2]	

Group - B

Answer **any five** questions

 $[5\times10]$

[4]

[6]

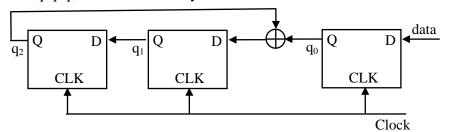
[4]

[2]

[3]

7. a) Consider the following circuit where ⊕ represents Exclusive OR. The D flip-flops are initialized to zeros.

The following data 100110000 is supplied to the data terminal in nine clock cycles. What will be the values of $q_2q_1q_0$ after nine clock cycles?



- b) Design a full adder using 4×1 MUX keeping the MSB fixed.
- 8. a) Design a combinational circuit for 2 4 2 1 to BCD conversion. [8]
 - b) What is the advantage of Carry-Lookahead adder? [2]
- 9. a) Explain the operation of a 3 bit PISO Shift Left register with proper diagram. [3+3]
 - b) Compare Control Flow and Data Flow architecture.
- 10. a) Compare Static and Dynamic RAM. [4]
 - b) Draw the USB topology diagram and explain USB system overview. [4]
 - c) Differentiate between counter and register.
- 11. a) Explain Indexed addressing and Immediate addressing with proper example. [4]
 - b) Explain the role of various address registers. [3]
 - c) Why are multiplexers called functionally complete block? [3]
- 12. a) Design a mod-6 asynchronous counter using D flip flop. [4]
- b) Draw and explain a single bus datapath of control unit and show the sequence of control signals for the instruction Move (R1), R2.
- for the instruction Move (R1), R2. [6]
- 13. a) Explain asynchronous inputs of flip-flop in brief. [2]
 - b) Draw the logic diagram of a Master-Slave JK flip flop using only NAND gates with asynchronous inputs.
 - c) Suppose physical addresses are 32 bit long. Cache contains 256K words of data and each block contains 4 words. Specify how the 32 bit address would be partitioned for each of the following configurations: (i) Direct mapped (ii) Associative [5]
- 14. a) Draw and explain the basic components of a microprogrammed control unit. [5]
 - b) Explain different types of cache miss techniques. [5]

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